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On

May 1, 2006

TOWNSEND and TOWNSEND and CREW LLP

By:

Eleonor J. Taylor

PATENT

Attorney Docket No.: 018419-008320US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**IN THE UNITED STATES PATENT
AND TRADEMARK OFFICE**

In re application of:

SIEN G. KANG et al.

Application No.: 09/893,340

Filed: June 26, 2001

For: SURFACE FINISHING OF SOI
SUBSTRATES USING AN EPI
PROCESS

Customer No.: 20350

Confirmation No. 2640

Examiner: Jack S.J. Chen

Technology Center/Art Unit: 2813

DECLARATION OF SIEN G. KANG
UNDER 37 CFR §1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I declare as follows:

1. I am a co-inventor of the above-referenced patent application. I have extensive experience and education in the field of manufacturing semiconductor substrates. Based upon my training, I do not think one of ordinary skill in the art of manufacturing semiconductor substrates, would have been motivated to combine the prior art references relied upon by the

Examiner to reject the claims pending in the instant application. In particular, I do not believe that one of ordinary skill would have found suggestion to combine the Ohshima Patent and Moriceau Article references dealing with manufacture of substrates, with the Benton Patent dealing with the fabrication of devices in semiconducting chips. The basis for my conclusion is provided below.

2. My formal education is as a chemical engineer. In 1979 received my Bachelor of Science degree in Chemical Engineering at the University of Lowell in Lowell, Massachusetts. In 1983 I received a Master's degree in Chemical Engineering from Pennsylvania State University in University Park, Pennsylvania.

3. I have extensive experience working for Silicon Genesis Corporation ("SiGen") in the field of manufacturing semiconductor substrates. SiGen is a manufacturer of semiconductor substrates formed from multiple layers of material, for example silicon-on-insulator (SOI) substrates such as silicon-on-oxide, silicon-on-sapphire, and silicon-on-quartz. Examples of other types of multi-layer semiconductor substrates include silicon-on-germanium, and silicon-on-silicon. I am currently employed by SiGen as an Integration Manager, where my duties include overseeing the work of the engineers responsible for fabricating and testing the quality of different types of multilayer substrates. Prior to working as an Integration Manager, since 1998 I worked for SiGen first as a Project Engineer, and then as a Project Manager.

4. Prior to joining SiGen in 1998, I had over eleven years worth of experience in the semiconductor industry. For example, from 1996-1998, I was a Senior Member of the Technical Staff for the Institute of Microelectronics (IME) located in Singapore. In this position, my duties included preparing metallization tools for operation in a newly-constructed fabrication facility. For ten years prior to joining IME, from 1986-1996 I worked in various process engineering positions for Genus, Inc. of Sunnyvale, California, where my job duties included the design of tools for use in depositing tungsten-containing materials such as tungsten nitride and tungsten silicide. From 1984-1986, I was employed by Intel Corp. as a Process Engineer, where my

duties included line operation of a semiconductor device tool utilized in formation of layers of metallization in a memory device.

5. I have reviewed in detail the following materials relating to prosecution of the instant patent application:

- a. Office Action including Final Rejection of Claims Mailed November 2, 2005, attached hereto as Exhibit A;
- b. U.S. Patent 6,251,754 to Ohshima et al. ("the Ohshima Patent") relied upon by the Examiner in the Office Action of November 2, 2005 and attached hereto as Exhibit B;
- c. U.S. Patent No. 5,141,878 to Benton et al. ("the Benton Patent") relied upon by the Examiner in the Office Action of November 2, 2005 and attached hereto as Exhibit C;
- d. Moriceau et al., "Hydrogen annealing treatment used to obtain high quality SOI surfaces", IEEE Intl'l SOI Conference Proceedings 37-38 (1998) ("the Moriceau Article") relied upon by the Examiner in the Office Action of November 2, 2005 and attached hereto as Exhibit D;

I understand that the Examiner has rejected many of the pending claims of the instant application as obvious based upon the Ohshima Patent in combination with the Moriceau article and the Benton Patent.

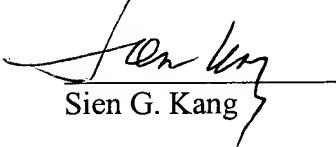
6. Based upon my experience and training, I do not believe that one of ordinary skill in the art of manufacturing semiconductor substrates, would have been motivated to combine the reference teachings relied upon by the Examiner in order to devise the claimed invention. In particular, both the Ohshima Patent and the Moriceau Article specifically relate to the field of manufacturing semiconductor substrates. The Ohshima Patent describes a method of manufacturing a semiconductor substrate, and the Moriceau Article describes a method of treating a surface of a substrate. By contrast, the Benton Patent relates to the field of fabricating active devices on semiconductor chips. In particular, the Benton Patent describes fabrication of a photodiode structure on a silicon substrate that has already been manufactured and provided. Because of the substantially different fields (i.e. substrate manufacture vs. chip fabrication)

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implicated by the Ohshima Patent/Moriceau Article and the Benton Patent, I do not believe that one of skill in the art would have been motivated to combine these references.

I hereby declare that all statements made herein of my own knowledge are true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.


Sien G. Kang

4/27/06
Dated

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